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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,201	08/24/2005	Helmut Tews	10808/192	4891

7590 03/31/2006

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EXAMINER	
AHMADI, MOHSEN	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/519,201	TEWS, HELMUT	
	Examiner	Art Unit	
	Mohsen Ahmadi	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9,13-16 and 21* is/are rejected.

7)☒ Claim(s) *5-8,11,12,17-20,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/17/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application number 10/519,201 for a "Method For Producing a Spacer Structure" field June 17, 2002 has been examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 9, 13, 15 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chien et al. (US Pat. 6,319,839).

Regarding claims 1 and 13, Figure 4, of Chien et al. shows forming a gate insulation layer (11,12 and 111) having a gate deposition inhibiting layer 12 (nitride), a gate layer 13 (polysilicon) and a covering deposition-inhibiting layer 44 on a semiconductor substrate 10. Figure 4, of Chien et al. also shows how the gate layer 13 and the covering deposition-inhibiting layer 44 have been patterned in order to form gate stack. Figure 7, of Chien et al. shows depositing an insulation layer 60, with respect to the deposition-inhibiting layer to form the pacer structure, Figure. 7 of Chien et al. shows the slight oxide growth at the horizontal surface of the deposition inhibiting layer 12 (nitride) and layer 44 and high oxide growth at the sidewalls of the gate oxide. Chien et al. does not disclose selective deposition. It would have been obvious to one

of ordinary skill in the art, to select the different range of an insulation layer 60 on the horizontal surface of the deposition-inhibiting layer 12 and the side walls of the gate stack in order to form the spacer structure (See cols. 2 and 3 lines 52-67 and 1-48) which would be considered as a selective deposition by one of ordinary skill in the art.

Regarding claims 3 and 15, Figure 9, of Chien et al. shows depositing a further insulation layer 90, selectively with respect to the deposition-inhibiting layer in order to form a widened spacer structure. Figure 9, of Chien et al. shows the slight oxide growth at the horizontal surface of the deposition-inhibiting layer 12 (nitride) and layer 44 and high oxide growth at the sidewalls of the gate oxide. It would have been obvious to one of ordinary skill in the art, to select high oxide at the sidewalls of the gate oxide and slight oxide at the horizontal surface of the deposition- inhibiting layer in order to form a widened spacer structure.

Regarding claims 9 and 21, Chien et al. discloses a method wherein the gate layer 13, includes polycrystalline silicon and the semiconductor substrate includes crystalline silicon (See col. 2 lines 43-67).

Claims 2, 4, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chien et al. (US Pat. 6,319,839) in view of Tseng (US Pat. 6,258,682).

Regarding claims 2, 4, 14 and 16, Chien et al. discloses all of the claimed features as stated above except for the carrying out an implantation in order to form connection doping regions and source and drain regions in the semiconductor substrate.

Tseng discloses a method of fabricating ultra shallow junction MOSFET. Tseng also discloses forming sidewall spacers using anisotropic etching.

Tseng discloses carrying out an implantation in order to form connection doping regions and source and drain regions in the semiconductor substrate (See col. 3 lines 16-25).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the connection doping regions and source and drain regions as disclosed by Tseng in the process of Chien et al. for it's known benefit as disclosed by Tseng, performing a silicide process to form silicide layer on the source/drain regions and activate the conductive impurities to form deep junction (See abstract).

Allowable Subject Matter

Claims 5-8, 11-12, 17-20 and 22-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The cited prior art does not disclose or suggest wherein the deposition inhibiting layer include high nitrogen content and ozone-enhanced TEOS deposition which is carried out in C, and wherein the deposition inhibiting layer have thin residual layers and

removing the residual layers by wet etching and densifying the selectively deposited insulation layer and depositing a material which can be silicided.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsen Ahmadi whose telephone number is 1-571-272-5062. The examiner can normally be reached on Mon-Fri 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 1-571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MA Mohsen Ahmadi
03/21/2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER